SKYNEX ACADEMY · ANALOG AND DIGITAL SYSTEMS

Digital Electronics Exercise Book

266 logic exercises, from number systems to PLC programming. Write your answer in the box under each question: the box turns **green** when it is correct and **red** when it is wrong. 206 questions are checked automatically; for the others, compare with the answer and mark yourself.

Chapter 1

Number systems and codes

Binary, octal and hexadecimal numbers, binary arithmetic, signed numbers and the codes used inside digital equipment.

1.1 Binary and decimal

Key ideas

- Each binary place is worth twice the place on its right: …, 16, 8, 4, 2, 1 . ½, ¼, ⅛, …
- Decimal → binary: divide by 2 again and again and read the remainders from the bottom up.
- Decimal fraction → binary: multiply the fraction by 2 again and again and read the whole-number parts from the top down.
- With n bits you can count from 0 to $2^n - 1$.

1.1.1 Basic

Convert these binary numbers to decimal:

(a) $(1011)_2$

(b) $(11010)_2$

(c) $(100111)_2$

(d) $(11111111)_2$

YOUR ANSWER

(a) number (b) number

(c) number (d) number

1.1.2 Basic

Convert these decimal numbers to binary:

(a) $(19)_{10}$

(b) $(46)_{10}$

(c) $(100)_{10}$

(d) $(255)_{10}$

YOUR ANSWER

(a) binary, e.g. 1011 (b) binary, e.g. 1011

(c) binary, e.g. 1011 (d) binary, e.g. 1011

1.1.3 Basic

Show every step of converting 46 to binary by repeated division by 2.

YOUR ANSWER

46 in binary binary, e.g. 1011

1.1.4 Practice

Convert these binary numbers (with fractions) to decimal:

(a) $(101.11)_2$

(b) $(1100.011)_2$

(c) $(0.1011)_2$

YOUR ANSWER

(a) number (b) number

(c) number

1.1.5 Practice

Convert to binary (give at most 6 bits after the point):

(a) $(6.75)_{10}$

(b) $(13.625)_{10}$

(c) $(0.3)_{10}$

YOUR ANSWER

(a) binary, e.g. 1011 (b) binary, e.g. 1011

(c) binary, e.g. 1011

1.1.6 Basic

What is the largest decimal number you can write with (a) 6 bits (b) 8 bits (c) 12 bits?

YOUR ANSWER

(a) number (b) number

(c) number

1.1.7 Practice

How many bits are needed to write (a) 1000 (b) 5000 (c) 65 535 in binary?

YOUR ANSWER

(a) number (b) number

(c) number

1.1.8 Challenge

A sensor sends a reading as 10 bits. (a) How many different values can it send? (b) If 0 means 0 °C and the largest value means 100 °C, what temperature does the reading 1000000000 stand for?

YOUR ANSWER

(a) values number (b) temperature e.g. 1.5 k°C

1.2 Octal and hexadecimal

Key ideas

- Octal uses the digits 0–7; one octal digit = 3 bits.
- Hexadecimal uses 0–9 and A–F (A = 10 … F = 15); one hex digit = 4 bits.
- Binary → octal/hex: group the bits in 3s or 4s starting from the point, adding zeros at the ends if needed.

1.2.1 Basic

Convert these octal numbers to decimal:

(a) $(57)_8$

(b) $(144)_8$

(c) $(777)_8$

(d) $(1750)_8$

YOUR ANSWER

(a) number (b) number

(c) number (d) number

1.2.2 Basic

Convert these decimal numbers to octal:

(a) $(100)_{10}$

(b) $(365)_{10}$

(c) $(1000)_{10}$

YOUR ANSWER

(a) octal (b) octal

(c) octal

1.2.3 Basic

Convert these binary numbers to octal:

(a) $(101110)_2$

(b) $(11011011)_2$

(c) $(1101.0111)_2$

YOUR ANSWER

(a) octal (b) octal

(c) octal

1.2.4 Basic

Convert these octal numbers to binary:

(a) $(47)_8$

(b) $(362)_8$

(c) $(7.25)_8$

YOUR ANSWER

(a) binary, e.g. 1011 (b) binary, e.g. 1011

(c) binary, e.g. 1011

1.2.5 Basic

Convert these hexadecimal numbers to decimal:

(a) $(2F)_{16}$

(b) $(A0)_{16}$

(c) $(3E8)_{16}$

(d) $(FFFF)_{16}$

YOUR ANSWER

(a) number (b) number

(c) number (d) number

1.2.6 Basic

Convert these decimal numbers to hexadecimal:

(a) $(75)_{10}$

(b) $(255)_{10}$

(c) $(4096)_{10}$

(d) $(2025)_{10}$

YOUR ANSWER

(a) hex, e.g. 3F (b) hex, e.g. 3F

(c) hex, e.g. 3F (d) hex, e.g. 3F

1.2.7 Basic

Convert these binary numbers to hexadecimal:

(a) $(11010110)_2$

(b) $(101111100101)_2$

(c) $(1110.1011)_2$

YOUR ANSWER

(a) hex, e.g. 3F (b) hex, e.g. 3F

(c) hex, e.g. 3F

1.2.8 Basic

Convert these hexadecimal numbers to binary:

(a) $(7C)_{16}$

(b) $(B3F)_{16}$

(c) $(1A.8)_{16}$

YOUR ANSWER

(a) binary, e.g. 1011 (b) binary, e.g. 1011

(c) binary, e.g. 1011

1.2.9 Practice

Convert $(3F7)_{16}$ to octal by going through binary.

YOUR ANSWER

in octal octal

1.2.10 Practice

Convert $(2735)_8$ to hexadecimal.

YOUR ANSWER

in hex hex, e.g. 3F

1.2.11 Challenge

A memory chip uses the addresses 0000_{16} to $3FFF_{16}$. (a) How many memory locations does it have? (b) How many address lines (bits) does it need?

YOUR ANSWER

(a) locations number (b) address lines number

1.2.12 Challenge

Web colours are written as three hex bytes: #RRGGBB. Give the red, green and blue values in decimal for (a) #FF8000 (b) #1E90FF.

YOUR ANSWER

(a) R number (a) G number

(a) B number (b) R number

(b) G number (b) B number

1.3 Binary arithmetic

Key ideas

- Addition: 0+0 = 0, 0+1 = 1, 1+1 = 0 carry 1, 1+1+1 = 1 carry 1.
- Subtraction: 0−0 = 0, 1−0 = 1, 1−1 = 0, 0−1 = 1 borrow 1.
- Multiplication and division work like in decimal, but every partial product is either 0 or the number itself.

1.3.1 Basic

Add:

(a) 1011 + 0110

(b) 11101 + 10111

(c) 1011.01 + 110.11

(d) 1111 + 1111

YOUR ANSWER

(a) binary, e.g. 1011 (b) binary, e.g. 1011

(c) binary, e.g. 1011 (d) binary, e.g. 1011

1.3.2 Basic

Subtract:

(a) 1101 − 0110

(b) 101000 − 10011

(c) 1100.1 − 11.11

YOUR ANSWER

(a) binary, e.g. 1011 (b) binary, e.g. 1011

(c) binary, e.g. 1011

1.3.3 Practice

Multiply:

(a) 1011 × 101

(b) 1101 × 110

(c) 111 × 111

YOUR ANSWER

(a) binary, e.g. 1011 (b) binary, e.g. 1011

(c) binary, e.g. 1011

1.3.4 Practice

Divide:

(a) 110110 ÷ 110

(b) 1111000 ÷ 1010

(c) 1010001 ÷ 1001

YOUR ANSWER

(a) binary, e.g. 1011 (b) binary, e.g. 1011

(c) binary, e.g. 1011

1.3.5 Practice

Add the three numbers 1101 + 1011 + 111 and check your answer in decimal.

YOUR ANSWER

sum in binary binary, e.g. 1011

1.3.6 Challenge

Multiplying a binary number by 2 shifts it one place to the left. What do you get when you shift 0010 1101 (a) one place left (b) two places right? Give the decimal values too.

YOUR ANSWER

(a) binary binary, e.g. 1011 (b) binary binary, e.g. 1011

1.4 Complements and signed numbers

Key ideas

- 1's complement: change every 0 into 1 and every 1 into 0.
- 2's complement: the 1's complement plus 1. It is how computers store negative numbers.
- In n-bit 2's complement the left bit is the sign (0 = +, 1 = –) and the range is -2^{n-1} to $+2^{n-1} - 1$.
- A – B = A + (2's complement of B); ignore the carry out of the left-most bit.

1.4.1 Basic

Give the 1's complement of:

(a) 1011

(b) 01101100

(c) 11110000

YOUR ANSWER

(a) e.g. 0110 (b) e.g. 0110

(c) e.g. 0110

1.4.2 Basic

Give the 2’s complement of:

(a) 0101

(b) 00011010

(c) 10000000

(d) 11111111

YOUR ANSWER

(a) e.g. 0110 (b) e.g. 0110

(c) e.g. 0110 (d) e.g. 0110

1.4.3 Basic

Write these numbers in 8-bit 2’s complement:

(a) +37

(b) –37

(c) –100

(d) –1

(e) –128

YOUR ANSWER

(a) e.g. 0110 (b) e.g. 0110

(c) e.g. 0110 (d) e.g. 0110

(e) e.g. 0110

1.4.4 Practice

What decimal values do these 8-bit 2's complement numbers stand for?

(a) 00101101

(b) 11010011

(c) 10000001

(d) 11111110

YOUR ANSWER

(a) number (b) number

(c) number (d) number

1.4.5 Practice

Use the 2's complement method to work out (8 bits): (a) 45 – 19 (b) 25 – 40 (c) –20 – 30.

YOUR ANSWER

(a) number (b) number

(c) number

1.4.6 Practice

Use 1's complement subtraction (with end-around carry) to work out 1011 – 0110.

YOUR ANSWER

result (binary) binary, e.g. 1011

1.4.7 Basic

What is the range of numbers you can store in (a) 8-bit (b) 16-bit 2’s complement?

YOUR ANSWER

(a) smallest number (a) largest number

(b) smallest number (b) largest number

1.4.8 Challenge

Add the 8-bit signed numbers 01110000 and 00110000. Is the answer correct? Explain what happened.

YOUR ANSWER

8-bit result e.g. 0110 Is it correct? (yes/no) answer

1.5 Binary codes: BCD, Excess-3, Gray and ASCII

Key ideas

- BCD (8421): every decimal digit is written as its own 4-bit group. 1010 to 1111 are not used.
- Excess-3: every digit is written as (digit + 3) in 4 bits. It is self-complementing.
- Gray code: only one bit changes between two neighbouring numbers. G = B $\oplus$ (B shifted right by one).
- ASCII: a 7-bit code for letters, digits and signs, e.g. ‘A’ = 65 = 41_{16}.

1.5.1 Basic

Write in BCD:

(a) 59

(b) 306

(c) 2025

YOUR ANSWER

(a) e.g. 0110 (b) e.g. 0110

(c) e.g. 0110

1.5.2 Basic

Decode these BCD numbers:

(a) 1001 0011

(b) 0111 0000 0110

(c) 0001 0101 1000 0100

YOUR ANSWER

(a) number (b) number

(c) number

1.5.3 Practice

Compare the binary and BCD forms of 97. Which needs more bits?

YOUR ANSWER

binary binary, e.g. 1011 BCD e.g. 0110

needs more bits answer

1.5.4 Basic

Is 0110 1101 a valid BCD number? Explain.

YOUR ANSWER

valid? (yes/no) answer

1.5.5 Challenge

Add 47 + 35 in BCD. Show the correction step.

YOUR ANSWER

BCD sum e.g. 0110

1.5.6 Basic

Write in Excess-3:

(a) 4

(b) 27

(c) 905

YOUR ANSWER

(a) e.g. 0110 (b) e.g. 0110

(c) e.g. 0110

1.5.7 Practice

Decode the Excess-3 number 0110 1001 1011.

YOUR ANSWER

decimal number

1.5.8 Challenge

Show that Excess-3 is self-complementing using the digit 2.

YOUR ANSWER

Excess-3 of 2 e.g. 0110 Excess-3 of 7 e.g. 0110

1.5.9 Basic

Convert binary to Gray code:

(a) 0110

(b) 1011

(c) 1111

(d) 10010

YOUR ANSWER

(a) e.g. 0110 (b) e.g. 0110

(c) e.g. 0110 (d) e.g. 0110

1.5.10 Basic

Convert Gray code to binary:

(a) 1101

(b) 1000

(c) 0111

YOUR ANSWER

(a) e.g. 0110 (b) e.g. 0110

(c) e.g. 0110

1.5.11 Practice

Write the full 3-bit Gray code sequence from 0 to 7.

YOUR ANSWER

Gray codes 0 → 7 e.g. 0110

1.5.12 Practice

Why is Gray code used in rotary position encoders?

YOUR ANSWER

Write your answer here, then compare it with the answer.

1.5.13 Basic

Give the ASCII code of the letters S, K and Y in decimal, hex and 7-bit binary.

YOUR ANSWER

S decimal	number	S hex	hex, e.g. 3F
K decimal	number	K hex	hex, e.g. 3F
Y decimal	number	Y hex	hex, e.g. 3F

1.5.14 Practice

What is the difference between the ASCII codes of ‘a’ and ‘A’? How can a program change a lowercase letter into a capital?

YOUR ANSWER

difference number

1.5.15 Practice

The character ‘7’ and the number 7 are not the same in a computer. Give both in binary.

YOUR ANSWER

number 7 binary, e.g. 1011 character ‘7’ binary, e.g. 1011

Chapter 2

Logic gates

The basic gates, their truth tables and symbols, universal gates and tristate outputs.

2.1 Basic gates and truth tables

Key ideas

- NOT: Y = A'. AND: Y = A·B (1 only if all inputs are 1). OR: Y = A + B (1 if any input is 1).
- NAND = AND followed by NOT; NOR = OR followed by NOT.
- XOR: Y = A ⊕ B = A'B + AB' (1 when the inputs are different). XNOR: 1 when the inputs are equal.
- A gate with n inputs has 2^n rows in its truth table.

2.1.1 Basic

Write the truth table of a 2-input AND, OR, NAND, NOR, XOR and XNOR gate in one table.

YOUR ANSWER

AND column e.g. 0110 OR column e.g. 0110

NAND column e.g. 0110 NOR column e.g. 0110

XOR column e.g. 0110 XNOR column e.g. 0110

2.1.2 Basic

Write the truth table of a 3-input NAND gate and a 3-input NOR gate.

YOUR ANSWER

NAND column e.g. 0110 NOR column e.g. 0110

2.1.3 Basic

How many rows does the truth table of a 5-input AND gate have? In how many of them is the output 1?

YOUR ANSWER

rows number rows with output 1 number

2.1.4 Practice

Two signals are sampled at 8 moments: A = 11001010, B = 10100110. Give the output of (a) AND (b) OR (c) XOR (d) NAND for each moment.

YOUR ANSWER

(a) e.g. 0110 (b) e.g. 0110

(c) e.g. 0110 (d) e.g. 0110

2.1.5 Practice

A gate gives these outputs for AB = 00, 01, 10, 11: 1, 0, 0, 0. Which gate is it? And for 0, 1, 1, 0?

YOUR ANSWER

1, 0, 0, 0 answer 0, 1, 1, 0 answer

2.1.6 Basic

Name the TTL chip that holds each of these: four 2-input NAND gates, six NOT gates, four 2-input AND gates, four 2-input OR gates, four 2-input XOR gates, four 2-input NOR gates.

YOUR ANSWER

NAND answer NOT answer

AND answer OR answer

XOR answer NOR answer

2.1.7 Challenge

A NAND gate has inputs A and B. Its output goes to a NOR gate together with input C. Write the expression for the output Y and its truth table.

YOUR ANSWER

Y = e.g. AB' + C

2.2 Negative-AND, Negative-OR, XOR uses and the INHIBIT gate

Key ideas

- Negative-AND (inputs inverted, then AND) = NOR. Negative-OR = NAND (De Morgan).
- XOR gives the parity of its inputs: the output is 1 when an odd number of inputs are 1.
- INHIBIT gate: Y = A·B'. Input B blocks (inhibits) A.

2.2.1 Basic

Show with a truth table that a Negative-AND gate (A'·B') behaves like a NOR gate.

YOUR ANSWER

A'·B' column e.g. 0110

2.2.2 Basic

Show with a truth table that a Negative-OR gate (A' + B') behaves like a NAND gate.

YOUR ANSWER

A' + B' column e.g. 0110

2.2.3 Practice

An even-parity bit is added to 7-bit data so the total number of 1s is even. Find the parity bit for:

(a) 1011000

(b) 1110111

(c) 0110100

(d) 1000001

YOUR ANSWER

(a) number (b) number

(c) number (d) number

2.2.4 Practice

Which gate can you use to check whether two bits are equal? Draw the idea for comparing two 2-bit numbers A1A0 and B1B0.

YOUR ANSWER

gate [answer]

2.2.5 Basic

Write the truth table of an INHIBIT gate Y = A·B'. What does input B do?

YOUR ANSWER

Y column [e.g. 0110]

2.2.6 Challenge

A machine motor M may only run when the start switch S is on and the safety guard G is NOT open (G = 1 means open). Which gate do you need? Write the expression.

YOUR ANSWER

gate [answer] M = [e.g. AB' + C]

2.3 Universal gates and tristate logic

Key ideas

- NAND and NOR are universal: any logic circuit can be built with only NAND gates or only NOR gates.
- A tristate (three-state) output can be 0, 1 or Z (high impedance, disconnected). The enable input decides.
- Several tristate outputs can share one bus wire, but only one may be enabled at a time.

2.3.1 Basic

Show how to make a NOT gate from (a) one NAND gate (b) one NOR gate.

YOUR ANSWER

Write your answer here, then compare it with the answer.

2.3.2 Practice

Build a 2-input AND gate and a 2-input OR gate using only NAND gates. How many gates does each need?

YOUR ANSWER

NAND gates for AND number NAND gates for OR number

2.3.3 Practice

Build a 2-input OR gate and a 2-input AND gate using only NOR gates.

YOUR ANSWER

NOR gates for OR number

NOR gates for AND number

2.3.4 Challenge

Build an XOR gate from four 2-input NAND gates. Give the output of each gate.

YOUR ANSWER

Write your answer here, then compare it with the answer.

2.3.5 Basic

A tristate buffer has data input A and active-high enable E. Write its truth table.

YOUR ANSWER

Y for EA = 00, 01, 10, 11 e.g. 0110

2.3.6 Practice

Two tristate buffers drive the same bus wire. Buffer 1 outputs 1 and buffer 2 outputs 0, and both are enabled. What happens, and how is it avoided?

YOUR ANSWER

Write your answer here, then compare it with the answer.

Chapter 3

Boolean algebra and Karnaugh maps

The laws of Boolean algebra, SOP and POS forms, minterms and maxterms, and simplification with Karnaugh maps.

3.1 Laws and algebraic simplification

Key ideas

- A + 0 = A, A·1 = A, A + 1 = 1, A·0 = 0, A + A = A, A·A = A, A + A' = 1, A·A' = 0, (A')' = A.
- Absorption: A + AB = A, A(A + B) = A, A + A'B = A + B.
- Distributive: A(B + C) = AB + AC and A + BC = (A + B)(A + C).
- De Morgan: (A + B)' = A'B' and (AB)' = A' + B'.

3.1.1 Basic

Name the law used in each line: (a) A + 1 = 1 (b) A·A' = 0 (c) A + AB = A (d) (AB)' = A' + B' (e) A(B + C) = AB + AC

YOUR ANSWER

Write your answer here, then compare it with the answer.

3.1.2 Basic

Simplify: Y = AB + AB' + A'B

YOUR ANSWER

Y = e.g. AB' + C

3.1.3 Basic

Simplify: Y = A + AB

YOUR ANSWER

Y = e.g. AB' + C

3.1.4 Basic

Simplify: Y = A(A + B)

YOUR ANSWER

Y = e.g. AB' + C

3.1.5 Basic

Simplify: Y = A + A'B

YOUR ANSWER

Y = e.g. AB' + C

3.1.6 Practice

Simplify: Y = (A + B)(A + C)

YOUR ANSWER

Y = e.g. AB' + C

3.1.7 Practice

Simplify: Y = AB + A'C + BC

YOUR ANSWER

Y = e.g. AB' + C

3.1.8 Practice

Simplify: Y = A'B'C + A'BC + AB'C + ABC

YOUR ANSWER

Y = e.g. AB' + C

3.1.9 Practice

Simplify: Y = (A + B')(A' + B)

YOUR ANSWER

Y = e.g. AB' + C

3.1.10 Practice

Simplify: Y = A'B'C' + A'BC' + AB'C' + ABC'

YOUR ANSWER

Y = e.g. AB' + C

3.1.11 Practice

Simplify: Y = ABC + ABC' + AB'C

YOUR ANSWER

Y = e.g. AB' + C

3.1.12 Practice

Use De Morgan’s theorem to write these without a bar over more than one letter: (a) (A + B + C)' (b) (AB + C)' (c) ((A + B)C')'

YOUR ANSWER

(a) e.g. AB' + C (b) e.g. AB' + C

(c) e.g. AB' + C

3.1.13 Challenge

Prove with algebra that AB + A'C + BC = AB + A'C (the consensus theorem).

YOUR ANSWER

Write your answer here, then compare it with the answer.

3.1.14 Practice

Check with a truth table that A + A'B = A + B.

YOUR ANSWER

A + A'B column e.g. 0110

A + B column e.g. 0110

3.2 SOP, POS, minterms and maxterms

Key ideas

- A minterm is an AND term that contains every variable once; it is 1 for exactly one row. m3 for ABC is A'BC.
- A maxterm is an OR term that is 0 for exactly one row. M3 for ABC is (A + B' + C').
- F = Σm(rows where F = 1) = ΠM(rows where F = 0).

3.2.1 Basic

Write the minterm and the maxterm for row 5 of a 3-variable truth table (A is the MSB).

YOUR ANSWER

m5 = e.g. AB' + C M5 = e.g. AB' + C

3.2.2 Basic

F(A, B, C) = Σm(1, 4, 6, 7). Write F as a canonical SOP expression and as a list of maxterms.

YOUR ANSWER

F (SOP) = e.g. AB' + C maxterm numbers e.g. a, b, c

3.2.3 Practice

Write the truth table of F(A, B, C) = Σm(0, 3, 5, 6). What simple gate circuit does it describe?

YOUR ANSWER

F column e.g. 0110 gate answer

3.2.4 Practice

Convert F(A, B, C, D) = ΠM(0, 2, 5, 7, 8, 10, 13, 15) into Σm form.

YOUR ANSWER

minterm numbers e.g. a, b, c

3.3 Karnaugh maps

Key ideas

- Rows and columns of a K-map are in Gray order (00, 01, 11, 10) so neighbours differ by one variable.
- Group the 1s in rectangles of 1, 2, 4, 8 or 16 cells; groups may wrap around the edges and may overlap.
- Make the groups as big as possible and use as few groups as possible.
- Group the 0s instead to get the POS form.

3.3.1 Basic

Use a 3-variable K-map to simplify F(A, B, C) = Σm(1, 3, 5, 7). Also give the POS form.

YOUR ANSWER

F = e.g. AB' + C

3.3.2 Basic

Use a 3-variable K-map to simplify F(A, B, C) = Σm(0, 2, 4, 6).

YOUR ANSWER

F = e.g. AB' + C

3.3.3 Basic

Use a 3-variable K-map to simplify F(A, B, C) = Σm(1, 2, 3, 7).

YOUR ANSWER

F = e.g. AB' + C

3.3.4 Basic

Use a 3-variable K-map to simplify F(A, B, C) = Σm(0, 1, 2, 4, 5).

YOUR ANSWER

F = e.g. AB' + C

3.3.5 Basic

Use a 3-variable K-map to simplify F(A, B, C) = Σm(2, 3, 4, 5, 6).

YOUR ANSWER

F = e.g. AB' + C

3.3.6 Practice

Use a 4-variable K-map to simplify F(A, B, C, D) = Σm(0, 1, 2, 5, 8, 9, 10).

YOUR ANSWER

F = e.g. AB' + C

3.3.7 Practice

Use a 4-variable K-map to simplify F(A, B, C, D) = Σm(4, 5, 6, 7, 12, 13, 14, 15).

YOUR ANSWER

F = e.g. AB' + C

3.3.8 Practice

Use a 4-variable K-map to simplify F(A, B, C, D) = Σm(0, 2, 5, 7, 8, 10, 13, 15).

YOUR ANSWER

F = e.g. AB' + C

3.3.9 Practice

Use a 4-variable K-map to simplify F(A, B, C, D) = Σm(1, 3, 4, 6, 9, 11, 12, 14).

YOUR ANSWER

F = e.g. AB' + C

3.3.10 Practice

Use a 4-variable K-map to simplify F(A, B, C, D) = Σm(0, 1, 3, 7, 8, 9, 11, 15).

YOUR ANSWER

F = e.g. AB' + C

3.3.11 Practice

Use a 4-variable K-map to simplify F(A, B, C, D) = Σm(2, 3, 6, 7, 10, 11, 13, 15).

YOUR ANSWER

F = e.g. AB' + C

3.3.12 Practice

Give the minimal POS form of F(A, B, C, D) = Σm(0, 1, 2, 3, 4, 6, 8, 9, 10, 11).

YOUR ANSWER

F (POS) = e.g. AB' + C

3.3.13 Challenge

Draw the 4-variable K-map of F = A'B'C'D' + A'B'CD' + AB'C'D' + AB'CD' and simplify it. Why is the answer so short?

YOUR ANSWER

F = e.g. AB' + C

3.4 Don’t-care conditions and design problems

Key ideas

- A don’t-care (x or d) is an input combination that never happens or whose output does not matter.
- Use a don’t-care as a 1 when it makes a group bigger; otherwise ignore it.
- BCD inputs 1010 to 1111 never happen, so they are don’t-cares.

3.4.1 Practice

Simplify F(A, B, C, D) = Σm(1, 3, 7, 11, 15) with don’t-cares d(0, 2, 5).

YOUR ANSWER

F = e.g. AB' + C

3.4.2 Practice

Simplify F(A, B, C, D) = Σm(0, 4, 8, 12) with don’t-cares d(2, 6, 10, 14).

YOUR ANSWER

F = e.g. AB' + C

3.4.3 Practice

Simplify F(A, B, C, D) = Σm(5, 6, 7) with don’t-cares d(10, 11, 12, 13, 14, 15).

YOUR ANSWER

F = e.g. AB' + C

3.4.4 Practice

Three judges vote with switches A, B and C. A lamp lights when at least two judges press their switch. Write the truth table and the simplest expression.

YOUR ANSWER

L = e.g. AB' + C

3.4.5 Challenge

A BCD digit ABCD drives a 7-segment display. Segment a (the top bar) is on for the digits 0, 2, 3, 5, 6, 7, 8 and 9. Find the simplest expression for segment a, using don’t-cares.

YOUR ANSWER

a = e.g. AB' + C

3.4.6 Challenge

Design a circuit with a BCD input ABCD whose output is 1 when the digit can be divided by 3 (0 counts as not divisible). Use don’t-cares.

YOUR ANSWER

F = e.g. AB' + C

3.4.7 Challenge

Implement F = AB + CD using only NAND gates.

YOUR ANSWER

NAND gates number

3.4.8 Practice

A car alarm Z sounds when the engine is off (E = 0) and either a door is opened (D = 1) or the glass breaks (G = 1). Write the expression and the truth table.

YOUR ANSWER

Z = e.g. AB' + C

Chapter 4

Combinational circuits

Adders, subtractors, comparators, multiplexers, demultiplexers, encoders and decoders.

4.1 Adders and subtractors

Key ideas

- Half adder: S = A ⊕ B, C = AB.
- Full adder: S = A ⊕ B ⊕ Cin, Cout = AB + Cin(A ⊕ B). Two half adders + an OR gate make a full adder.
- Half subtractor: D = A ⊕ B, Bout = A'B. Full subtractor: D = A ⊕ B ⊕ Bin, Bout = A'B + (A ⊕ B)'Bin.
- An XOR gate with a control input M is a controlled inverter: M = 0 passes B, M = 1 inverts B.

4.1.1 Basic

Write the truth table of a half adder and give the expressions for S and C.

YOUR ANSWER

S column e.g. 0110 C column e.g. 0110

S = e.g. AB' + C C = e.g. AB' + C

4.1.2 Basic

Write the truth table of a full adder.

YOUR ANSWER

S column e.g. 0110 Cout column e.g. 0110

4.1.3 Practice

Show that Cout = AB + Cin(A ⊕ B) is the same as the majority function AB + ACin + BCin.

YOUR ANSWER

Write your answer here, then compare it with the answer.

4.1.4 Practice

A 4-bit parallel adder (7483) adds A3A2A1A0 + B3B2B1B0 with carry-in C0. Find the sum and the carry out:

(a) A = 0101, B = 0011, C0 = 0

(b) A = 1001, B = 0111, C0 = 0

(c) A = 1111, B = 0001, C0 = 1

(d) A = 1100, B = 1010, C0 = 0

YOUR ANSWER

(a) S	e.g. 0110	(a) C4	number
(b) S	e.g. 0110	(b) C4	number
(c) S	e.g. 0110	(c) C4	number
(d) S	e.g. 0110	(d) C4	number

4.1.5 Basic

Write the truth table of a half subtractor (A − B).

YOUR ANSWER

D column e.g. 0110 Bout column e.g. 0110

4.1.6 Practice

Write the truth table of a full subtractor (A − B − Bin).

YOUR ANSWER

D column e.g. 0110 Bout column e.g. 0110

4.1.7 Challenge

A 4-bit adder–subtractor uses XOR gates on the B inputs and the mode line M as carry-in. Work out A − B for A = 0110, B = 0011 and for A = 0011, B = 0110. Explain the carry out.

YOUR ANSWER

(a) A − B number (b) A − B number

4.2 Comparators

Key ideas

- 1-bit comparator: (A > B) = AB', (A < B) = A'B, (A = B) = (A ⊕ B)'.
- A multi-bit comparator looks at the most significant bits first; the 7485 compares two 4-bit numbers and can be cascaded.

4.2.1 Basic

Write the truth table and the three output expressions of a 1-bit comparator.

YOUR ANSWER

A > B = e.g. AB' + C

A = B = e.g. AB' + C

A < B = e.g. AB' + C

4.2.2 Practice

Write the expression for A = B for two 2-bit numbers A1A0 and B1B0.

YOUR ANSWER

(A = B) = e.g. AB' + C

4.2.3 Practice

Give the 7485 outputs (A>B, A=B, A<B) for: (a) A = 1011, B = 1001 (b) A = 0110, B = 0110 (c) A = 0111, B = 1000

YOUR ANSWER

(a) e.g. 0110

(b) e.g. 0110

(c) e.g. 0110

4.2.4 Challenge

How do you connect two 7485 chips to compare two 8-bit numbers?

YOUR ANSWER

Write your answer here, then compare it with the answer.

4.3 Multiplexers and demultiplexers

Key ideas

- A multiplexer (MUX) connects one of 2^n data inputs to its output; n select lines choose which.
- Y of a 4-to-1 MUX = S1'S0'D0 + S1'S0D1 + S1S0'D2 + S1S0D3.
- Any function of n variables can be made with a 2^n-to-1 MUX (or a 2^{n-1}-to-1 MUX with the last variable on the data inputs).
- A demultiplexer (DEMUX) sends one input to one of 2^n outputs.

4.3.1 Basic

How many select lines do these multiplexers need: 4-to-1, 8-to-1, 16-to-1, 32-to-1?

YOUR ANSWER

4-to-1 number 8-to-1 number

16-to-1 number 32-to-1 number

4.3.2 Basic

An 8-to-1 MUX has D0…D7 = 1, 0, 0, 1, 1, 1, 0, 1. What is the output for S2S1S0 = 011, 101, 110?

YOUR ANSWER

011 number 101 number

110 number

4.3.3 Practice

Implement F(A, B, C) = Σm(1, 2, 6, 7) with an 8-to-1 MUX. What goes on each data input?

YOUR ANSWER

D0 … D7 e.g. 0110

4.3.4 Challenge

Implement the same function F(A, B, C) = Σm(1, 2, 6, 7) with a 4-to-1 MUX, using A and B as select lines.

YOUR ANSWER

D0 = answer D1 = answer

D2 = answer D3 = answer

4.3.5 Challenge

Implement F(A, B, C) = Σm(0, 2, 3, 5) with a 4-to-1 MUX (A, B on the select lines).

YOUR ANSWER

D0 = answer D1 = answer

D2 = answer D3 = answer

4.3.6 Basic

A 1-to-4 DEMUX has data input D = 1 and select S1S0 = 10. Which output is 1?

YOUR ANSWER

output answer

4.3.7 Practice

Write the four output expressions of a 1-to-4 demultiplexer.

YOUR ANSWER

Y0 = e.g. AB' + C Y1 = e.g. AB' + C

Y2 = e.g. AB' + C Y3 = e.g. AB' + C

4.4 Encoders and decoders

Key ideas

- An encoder turns one active input out of 2^n into an n-bit code. A priority encoder outputs the code of the highest active input.
- A decoder does the opposite: an n-bit code makes exactly one of 2^n outputs active. The 74LS138 is a 3-to-8 decoder with active-LOW outputs.
- A decoder plus an OR gate can make any function: OR together the outputs of its minterms.
- The 7447 decodes BCD for a common-anode 7-segment display.

4.4.1 Basic

Write the expressions of a 2-to-4 decoder with inputs A, B.

YOUR ANSWER

Y0 = e.g. AB' + C

Y1 = e.g. AB' + C

Y2 = e.g. AB' + C

Y3 = e.g. AB' + C

4.4.2 Basic

An 8-to-3 encoder has input 5 active. What are its outputs A2A1A0?

YOUR ANSWER

A2A1A0 e.g. 0110

4.4.3 Practice

A 4-to-2 priority encoder gets inputs D3D2D1D0 = 0110. What is the output? Which input wins?

YOUR ANSWER

output e.g. 0110 winning input answer

4.4.4 Practice

A 74LS138 has its enables active and CBA = 110. Give all eight outputs (they are active-LOW).

YOUR ANSWER

Y7 … Y0 e.g. 0110

4.4.5 Challenge

Build a full adder from a 3-to-8 decoder and two OR gates.

YOUR ANSWER

S: decoder outputs e.g. a, b, c Cout: decoder outputs e.g. a, b, c

4.4.6 Practice

Which segments of a 7-segment display light for the digits 2, 4 and 7?

YOUR ANSWER

digit 2 e.g. a, b, c

digit 4 e.g. a, b, c

digit 7 e.g. a, b, c

4.4.7 Challenge

Design a 3-bit binary-to-Gray converter. Give the expressions for G2, G1 and G0.

YOUR ANSWER

G2 = e.g. AB' + C

G1 = e.g. AB' + C

G0 = e.g. AB' + C

Chapter 5

Sequential logic and the 555 clock

Synchronous and asynchronous circuits, clock signals and how a 555 timer makes them.

5.1 Sequential circuits and clock signals

Key ideas

- A combinational circuit's output depends only on its present inputs; a sequential circuit also remembers its past (it has memory).
- Synchronous circuits change state only on a clock edge; asynchronous circuits change as soon as an input changes.
- Clock period T = 1/f. Duty cycle = time HIGH ÷ period × 100 %.

5.1.1 Basic

Give two differences between a combinational and a sequential circuit, with one example of each.

YOUR ANSWER

Write your answer here, then compare it with the answer.

5.1.2 Basic

Why are synchronous circuits used more often than asynchronous ones?

YOUR ANSWER

Write your answer here, then compare it with the answer.

5.1.3 Basic

A clock signal has a frequency of 25 kHz and is HIGH for 10 µs in each period. Find the period and the duty cycle.

YOUR ANSWER

period e.g. 1.5 ks duty cycle e.g. 1.5 k%

5.1.4 Practice

A clock has a period of 0.5 ms and a duty cycle of 60 %. How long is it HIGH and how long LOW? What is its frequency?

YOUR ANSWER

HIGH time e.g. 1.5 ks LOW time e.g. 1.5 ks

frequency e.g. 1.5 kHz

5.2 The 555 timer

Key ideas

- Pins: 1 GND, 2 trigger, 3 output, 4 reset, 5 control voltage, 6 threshold, 7 discharge, 8 +Vcc.
- Inside: two comparators (at ⅓ Vcc and ⅔ Vcc), an SR flip-flop, a discharge transistor and an output stage.
- Astable: tH = 0.693(RA + RB)C, tL = 0.693·RB·C, f = 1.44 / ((RA + 2RB)C), duty = (RA + RB)/(RA + 2RB).
- Monostable: one pulse of width T = 1.1·R·C each time pin 2 is pulled below ⅓ Vcc.

5.2.1 Basic

Name the eight pins of the 555 timer and say what pins 2, 4 and 6 do.

YOUR ANSWER

Write your answer here, then compare it with the answer.

5.2.2 Basic

With Vcc = 9 V, at what voltages do the two comparators of a 555 switch?

YOUR ANSWER

lower comparator e.g. 1.5 kV upper comparator e.g. 1.5 kV

5.2.3 Basic

A 555 astable has RA = 1 kΩ, RB = 10 kΩ and C = 10 µF. Find tH, tL, the frequency and the duty cycle.

YOUR ANSWER

tH e.g. 1.5 ks tL e.g. 1.5 ks

f e.g. 1.5 kHz duty cycle e.g. 1.5 k%

5.2.4 Basic

A 555 astable has RA = 4.7 kΩ, RB = 47 kΩ and C = 1 µF. Find tH, tL, the frequency and the duty cycle.

YOUR ANSWER

tH e.g. 1.5 ks tL e.g. 1.5 ks

f e.g. 1.5 kHz duty cycle e.g. 1.5 k%

5.2.5 Practice

A 555 astable has RA = 10 kΩ, RB = 10 kΩ and C = 100 nF. Find tH, tL, the frequency and the duty cycle.

YOUR ANSWER

tH e.g. 1.5 ks tL e.g. 1.5 ks

f e.g. 1.5 kHz duty cycle e.g. 1.5 k%

5.2.6 Practice

A 555 astable has RA = 2.2 kΩ, RB = 68 kΩ and C = 10 nF. Find tH, tL, the frequency and the duty cycle.

YOUR ANSWER

tH e.g. 1.5 ks

tL e.g. 1.5 ks

f e.g. 1.5 kHz

duty cycle e.g. 1.5 k%

5.2.7 Basic

A 555 monostable has R = 100 kΩ and C = 10 µF. How long is the output pulse?

YOUR ANSWER

pulse width e.g. 1.5 ks

5.2.8 Basic

A 555 monostable has R = 47 kΩ and C = 100 µF. How long is the output pulse?

YOUR ANSWER

pulse width e.g. 1.5 ks

5.2.9 Basic

A 555 monostable has R = 1 MΩ and C = 2.2 µF. How long is the output pulse?

YOUR ANSWER

pulse width e.g. 1.5 ks

5.2.10 Practice

Design a 555 astable that gives about 1 kHz with C = 100 nF and RA = 1 kΩ. Find RB.

YOUR ANSWER

RB e.g. 1.5 kΩ

5.2.11 Challenge

Why can a basic 555 astable never give a duty cycle of 50 % or less? How can a diode across RB fix this?

YOUR ANSWER

Write your answer here, then compare it with the answer.

5.2.12 Practice

You need a 10-second delay from a 555 monostable with C = 100 µF. Which resistor do you need?

YOUR ANSWER

R e.g. 1.5 kΩ

Chapter 6

Flip-flops

Latches and flip-flops: SR, clocked SR, D, JK, T and master–slave.

6.1 SR latch and clocked SR flip-flop

Key ideas

- A flip-flop stores one bit. Q is the stored bit and Q' its complement.
- SR: S = 1 sets Q to 1, R = 1 resets Q to 0, S = R = 0 holds, S = R = 1 is not allowed.
- A NAND latch has active-LOW inputs (S' and R'); a NOR latch has active-HIGH inputs.
- A clocked (gated) SR only reacts while the clock/enable is active.

6.1.1 Basic

Write the characteristic (truth) table of a clocked SR flip-flop.

YOUR ANSWER

Write your answer here, then compare it with the answer.

6.1.2 Basic

Why is S = R = 1 not allowed for a NOR SR latch?

YOUR ANSWER

Write your answer here, then compare it with the answer.

6.1.3 Practice

A clocked SR flip-flop starts with Q = 0. At each clock pulse the inputs (S, R) are: (1,0), (0,0), (0,1), (0,0), (1,0), (1,1). Give Q after each pulse.

YOUR ANSWER

Q after each pulse answer

6.1.4 Practice

Draw (describe) an SR latch made of two NAND gates and write its truth table.

YOUR ANSWER

Write your answer here, then compare it with the answer.

6.1.5 Challenge

Give the characteristic equation of the SR flip-flop and check it for S = 1, R = 0 and Q = 0.

YOUR ANSWER

Q^+ = e.g. AB' + C

6.2 D, JK and T flip-flops

Key ideas

- D: $Q^+ = D$. It removes the forbidden state of the SR by using S = D and R = D'.
- JK: like SR, but J = K = 1 toggles. $Q^+ = JQ' + K'Q$.
- T: T = 1 toggles, T = 0 holds. $Q^+ = T \oplus Q$. A JK with J = K = T is a T flip-flop.
- Edge-triggered flip-flops change only on the rising (↑) or falling (↓) clock edge.

6.2.1 Basic

Write the truth tables of the D, JK and T flip-flops.

YOUR ANSWER

Write your answer here, then compare it with the answer.

6.2.2 Basic

A rising-edge D flip-flop starts with Q = 0. D at each rising edge is 1, 1, 0, 1, 0, 0, 1. Give Q after each edge.

YOUR ANSWER

Q after each edge e.g. 0110

6.2.3 Practice

A JK flip-flop starts with Q = 0. The inputs (J, K) at each clock edge are (1,0), (1,1), (1,1), (0,0), (0,1), (1,1), (1,0). Give Q after each edge.

YOUR ANSWER

Q after each edge e.g. 0110

6.2.4 Practice

A T flip-flop starts with Q = 1. T at each clock edge is 1, 1, 0, 1, 1, 1, 0. Give Q after each edge.

YOUR ANSWER

Q after each edge e.g. 0110

6.2.5 Practice

Show how to turn (a) a JK flip-flop into a D flip-flop (b) a JK into a T flip-flop (c) a D flip-flop into a T flip-flop.

YOUR ANSWER

Write your answer here, then compare it with the answer.

6.2.6 Practice

Write the excitation tables of the JK, D and T flip-flops (the inputs needed for each change Q → Q^+).

YOUR ANSWER

Write your answer here, then compare it with the answer.

6.2.7 Challenge

Prove the JK characteristic equation $Q^+ = JQ' + K'Q$ from its truth table with a K-map.

YOUR ANSWER

$Q^+ =$ e.g. AB' + C

6.3 Master–slave flip-flops, preset and clear

Key ideas

- A master–slave flip-flop is two latches: the master follows the inputs while CLK = 1, the slave copies the master when CLK goes to 0.
- This stops the ‘race-around’ problem of a level-triggered JK with J = K = 1.
- Preset (PRE) and clear (CLR) are asynchronous inputs: they act at once, without waiting for the clock.

6.3.1 Basic

What is the race-around condition and how does the master–slave arrangement stop it?

YOUR ANSWER

Write your answer here, then compare it with the answer.

6.3.2 Practice

A 74LS76 JK flip-flop has active-LOW PRE and CLR. What is Q when (a) PRE = 0, CLR = 1 (b) PRE = 1, CLR = 0 (c) PRE = CLR = 1?

YOUR ANSWER

(a) Q number (b) Q number

6.3.3 Practice

Why do we say that preset and clear are asynchronous inputs?

YOUR ANSWER

Write your answer here, then compare it with the answer.

Chapter 7

Frequency division and counters

Dividing frequencies with toggle flip-flops, ripple and synchronous counters, up/down and presettable counters, cascading and counter design.

7.1 Frequency division

Key ideas

- A toggle flip-flop (D with D = Q', or JK with J = K = 1) changes state on every clock edge: its output frequency is f/2.
- n toggle flip-flops in a chain divide by 2^n.

7.1.1 Basic

How do you connect a D flip-flop so that it divides the clock frequency by 2?

YOUR ANSWER

Write your answer here, then compare it with the answer.

7.1.2 Basic

A 32.768 kHz watch crystal clock goes through a chain of toggle flip-flops. What is the frequency after (a) 1 (b) 5 (c) 15 flip-flops?

YOUR ANSWER

(a) e.g. 1.5 kHz (b) e.g. 1.5 kHz

(c) e.g. 1.5 kHz

7.1.3 Practice

How many toggle flip-flops are needed to turn 1 MHz into a frequency below 1 kHz? What frequency do you get?

YOUR ANSWER

flip-flops number frequency e.g. 1.5 kHz

7.1.4 Practice

A 50 Hz mains signal is shaped into a square wave and divided by 2 six times. What is the output frequency and period?

YOUR ANSWER

frequency e.g. 1.5 kHz period e.g. 1.5 ks

7.2 Ripple (asynchronous) counters

Key ideas

- In a ripple counter only the first flip-flop gets the clock; each next flip-flop is clocked by the previous output.
- n flip-flops count 0 to $2^n - 1$ (modulus 2^n).
- For a modulus $N < 2^n$, a NAND gate detects N and clears all flip-flops.
- Each stage adds its delay: the maximum clock frequency is about $1 / (n \times t_{pd})$.

7.2.1 Basic

How many flip-flops are needed for a counter of modulus (a) 8 (b) 10 (c) 60 (d) 100?

YOUR ANSWER

(a) number (b) number

(c) number (d) number

7.2.2 Basic

A 4-bit binary ripple counter starts at 0000. What does it show after (a) 9 (b) 16 (c) 37 clock pulses?

YOUR ANSWER

(a) e.g. 0110 (b) e.g. 0110

(c) e.g. 0110

7.2.3 Practice

Design a MOD-6 ripple counter. How many flip-flops do you need, and which outputs go to the reset NAND gate?

YOUR ANSWER

flip-flops number outputs to the NAND gate e.g. a, b, c

7.2.4 Practice

Design a MOD-10 ripple counter. How many flip-flops do you need, and which outputs go to the reset NAND gate?

YOUR ANSWER

flip-flops number outputs to the NAND gate e.g. a, b, c

7.2.5 Practice

Design a MOD-12 ripple counter. How many flip-flops do you need, and which outputs go to the reset NAND gate?

YOUR ANSWER

flip-flops number outputs to the NAND gate e.g. a, b, c

7.2.6 Practice

Design a MOD-5 ripple counter. How many flip-flops do you need, and which outputs go to the reset NAND gate?

YOUR ANSWER

flip-flops number outputs to the NAND gate e.g. a, b, c

7.2.7 Practice

Each flip-flop in a 4-bit ripple counter has a delay of 25 ns. What is the longest settling time and the highest safe clock frequency?

YOUR ANSWER

settling time e.g. 1.5 ks fmax e.g. 1.5 kHz

7.2.8 Challenge

Why does a ripple counter that goes from 0111 to 1000 show false states for a short time? Which false states can appear?

YOUR ANSWER

false states e.g. a, b, c

7.2.9 Practice

The 7490 is a decade counter and the 7493 a 4-bit binary counter. How do you get MOD-10 and MOD-16 from them?

YOUR ANSWER

Write your answer here, then compare it with the answer.

7.3 Synchronous, up/down and presettable counters

Key ideas

- In a synchronous counter every flip-flop gets the same clock. A flip-flop toggles when all lower bits are 1 (count up).
- fmax = 1 / (tpd of a flip-flop + tpd of the AND gates).
- An up/down counter toggles a stage when all lower bits are 1 (up) or all lower bits are 0 (down).
- A presettable counter (74190–74193) can be loaded with any starting value.

7.3.1 Basic

Give the J and K inputs of each stage of a 4-bit synchronous binary up-counter.

YOUR ANSWER

Write your answer here, then compare it with the answer.

7.3.2 Practice

In a synchronous counter each flip-flop has tpd = 20 ns and each AND gate 10 ns. What is the highest clock frequency? Compare it with a 4-bit ripple counter made of the same flip-flops.

YOUR ANSWER

synchronous fmax e.g. 1.5 kHz ripple fmax e.g. 1.5 kHz

7.3.3 Basic

A 4-bit up/down counter is at 0110. Write the next five states when counting (a) up (b) down.

YOUR ANSWER

(a) next five (up) e.g. 0110 (b) next five (down) e.g. 0110

7.3.4 Practice

A down counter starts at 0011. What does it show after 5 clock pulses?

YOUR ANSWER

after 5 pulses e.g. 0110

7.3.5 Practice

A 74193 is loaded with 1001 and then counts up. What does it show after 10 pulses? Which output tells you it passed 1111?

YOUR ANSWER

after 10 pulses e.g. 0110 output answer

7.3.6 Challenge

Use a presettable 4-bit counter to make a MOD-12 counter that counts from 4 to 15.

YOUR ANSWER

Write your answer here, then compare it with the answer.

7.4 Cascading counters

Key ideas

- Counters in cascade multiply their moduli: MOD-10 followed by MOD-6 = MOD-60.
- Two cascaded BCD (decade) counters count 00 to 99.

7.4.1 Basic

What is the total modulus of (a) a MOD-10 and a MOD-6 counter in cascade (b) three MOD-10 counters (c) MOD-16 and MOD-16?

YOUR ANSWER

(a) number (b) number

(c) number

7.4.2 Practice

A digital clock needs a 1 Hz pulse from a 1 kHz oscillator. Which counters do you cascade?

YOUR ANSWER

decade counters number

7.4.3 Practice

How do you build the seconds part (00–59) of a clock from counters?

YOUR ANSWER

Write your answer here, then compare it with the answer.

7.4.4 Challenge

Two cascaded BCD counters show 3 7. What do they show after 68 more pulses?

YOUR ANSWER

display shows number

7.5 Designing counters with any sequence

Key ideas

- 1. Draw the state diagram. 2. Make the state table (present state → next state).
- 3. Use the excitation table of the chosen flip-flop to find its inputs.
- 4. Simplify each input with a K-map (unused states are don’t-cares). 5. Draw the circuit.

7.5.1 Practice

Design a synchronous MOD-5 counter (0 → 4) with JK flip-flops.

YOUR ANSWER

J2 = e.g. AB' + C K2 = e.g. AB' + C

J1 = e.g. AB' + C K1 = e.g. AB' + C

J0 = e.g. AB' + C K0 = e.g. AB' + C

7.5.2 Challenge

Design a synchronous counter with JK flip-flops for the sequence 000 → 010 → 101 → 110 → 111 → 000 …

YOUR ANSWER

J2 = e.g. AB' + C K2 = e.g. AB' + C

J1 = e.g. AB' + C K1 = e.g. AB' + C

J0 = e.g. AB' + C K0 = e.g. AB' + C

7.5.3 Challenge

Design a synchronous counter with D flip-flops that counts only the odd numbers 1, 3, 5, 7.

YOUR ANSWER

D2 = e.g. AB' + C D1 = e.g. AB' + C

D0 = e.g. AB' + C

7.5.4 Challenge

Design a synchronous counter with T flip-flops for the sequence 000 → 001 → 011 → 111 → 110 → 100 → 000 …

YOUR ANSWER

T2 = e.g. AB' + C T1 = e.g. AB' + C

T0 = e.g. AB' + C

7.5.5 Practice

After designing a counter you must check the unused states. Why?

YOUR ANSWER

Write your answer here, then compare it with the answer.

Chapter 8

Shift registers and shift-register counters

SISO, SIPO, PISO, PIPO, bidirectional and universal shift registers, ring counters and Johnson counters.

8.1 Shift registers

Key ideas

- A shift register is a chain of D flip-flops with a common clock. Each pulse moves the data one place.
- SISO: serial in, serial out (a delay line). SIPO: serial in, parallel out. PISO: parallel in, serial out. PIPO: parallel in, parallel out.
- An n-bit SISO needs n clock pulses to load n bits and n more to read them out.
- A universal shift register (74194) can shift left, shift right, load in parallel or hold, chosen by S1S0.

8.1.1 Basic

Name the four kinds of shift register and give one use for SIPO and one for PISO.

YOUR ANSWER

Write your answer here, then compare it with the answer.

8.1.2 Basic

A 4-bit shift-right register holds 0000. The serial input gets 1, 0, 1, 1 (one bit per clock pulse). Give the contents after each pulse.

YOUR ANSWER

pulse 1 e.g. 0110 pulse 2 e.g. 0110

pulse 3 e.g. 0110 pulse 4 e.g. 0110

8.1.3 Practice

A 4-bit shift-right register holds 1010. The serial input gets 0, 1, 1, 0, 0. Give the contents after each pulse.

YOUR ANSWER

pulse 1 e.g. 0110 pulse 2 e.g. 0110

pulse 3 e.g. 0110 pulse 4 e.g. 0110

pulse 5 e.g. 0110

8.1.4 Basic

How many clock pulses do you need to load a byte into an 8-bit SIPO register? How many to read it out of a SISO register?

YOUR ANSWER

pulses to load number pulses in total for SISO (load + read) num

8.1.5 Practice

A SISO register has 8 stages and is clocked at 1 MHz. How long is a bit delayed between input and output?

YOUR ANSWER

delay e.g. 1.5 ks

8.1.6 Practice

The 74194 has mode inputs S1S0. What does it do for 00, 01, 10 and 11?

YOUR ANSWER

00 answer 01 answer

10 answer 11 answer

8.1.7 Challenge

A 4-bit register holds 0011 (= 3). What value does it hold after shifting left once and after shifting right twice (0s shifted in)? What arithmetic does this do?

YOUR ANSWER

after shifting left e.g. 0110 after shifting right twice e.g. 0110

8.2 Ring and Johnson counters

Key ideas

- Ring counter: Q of the last stage goes back to D of the first; one 1 circulates. n flip-flops → n states.
- Johnson (twisted-ring) counter: Q' of the last stage goes back; n flip-flops → 2n states.
- Each Johnson state can be decoded with one 2-input AND gate.

8.2.1 Basic

List the states of a 4-bit ring counter that starts at 1000.

YOUR ANSWER

the four states e.g. 0110

8.2.2 Basic

List the states of a 4-bit Johnson counter that starts at 0000.

YOUR ANSWER

the eight states e.g. 0110

8.2.3 Basic

How many states do you get from (a) a 5-bit ring counter (b) a 5-bit Johnson counter (c) a 5-bit binary counter?

YOUR ANSWER

(a) number (b) number

(c) number

8.2.4 Practice

You need a MOD-10 counter with outputs that never glitch. How many flip-flops does a Johnson counter need, and how many a ring counter?

YOUR ANSWER

Johnson flip-flops number ring flip-flops number

8.2.5 Practice

A 3-bit Johnson counter is clocked at 600 Hz. What is the frequency at each output?

YOUR ANSWER

output frequency e.g. 1.5 kHz

8.2.6 Challenge

Which two outputs must an AND gate use to decode the state 1100 of a 4-bit Johnson counter (sequence 0000, 1000, 1100, …)?

YOUR ANSWER

AND gate = e.g. AB' + C

Chapter 9

Logic families

TTL and CMOS, their sub-families and the parameters that describe a logic gate: voltage levels, noise margin, fan-out, delay and power.

9.1 Families and parameters

Key ideas

- TTL (bipolar transistors, 5 V): 74, 74LS, 74S, 74AS, 74ALS, 74F. CMOS (MOSFETs): 4000, 74HC, 74HCT, 74AC, 74LVC.
- Standard TTL: VIH = 2 V, VIL = 0.8 V, VOH = 2.4 V, VOL = 0.4 V.
- Noise margins: NMH = VOH − VIH and NML = VIL − VOL.
- Fan-out = the smaller of IOH/IIH and IOL/IIL.
- Speed–power product = propagation delay × power per gate (in pJ).

9.1.1 Basic

Name three TTL sub-families and three CMOS sub-families.

YOUR ANSWER

Write your answer here, then compare it with the answer.

9.1.2 Basic

Find the HIGH and LOW noise margins of standard TTL.

YOUR ANSWER

NMH e.g. 1.5 kV NML e.g. 1.5 kV

9.1.3 Practice

A 74HC gate at 5 V has VOH = 4.4 V, VIH = 3.5 V, VIL = 1.5 V, VOL = 0.1 V. Find its noise margins and compare them with TTL.

YOUR ANSWER

NMH e.g. 1.5 kV NML e.g. 1.5 kV

9.1.4 Basic

Standard TTL: IOH = 400 µA, IIH = 40 µA, IOL = 16 mA, IIL = 1.6 mA. What is the fan-out?

YOUR ANSWER

fan-out number

9.1.5 Practice

A 74LS gate has IOH = 400 µA, IOL = 8 mA, and each 74LS input needs IIH = 20 µA, IIL = 0.4 mA. How many 74LS inputs can it drive?

YOUR ANSWER

fan-out number

9.1.6 Challenge

A 74LS output (IOL = 8 mA, IOH = 400 µA) must drive standard 74 inputs (IIL = 1.6 mA, IIH = 40 µA). What is the fan-out?

YOUR ANSWER

fan-out number

9.1.7 Practice

A gate has tPLH = 11 ns and tPHL = 7 ns. What is its average propagation delay?

YOUR ANSWER

tpd e.g. 1.5 ks

9.1.8 Practice

A TTL chip with four gates draws ICCH = 8 mA and ICCL = 22 mA at 5 V. Find the average power per gate. With tpd = 10 ns, what is the speed–power product?

YOUR ANSWER

power per gate e.g. 1.5 kW speed–power product e.g. 1.5 kJ

9.1.9 Basic

Give two advantages of CMOS over TTL and one advantage of TTL.

YOUR ANSWER

Write your answer here, then compare it with the answer.

9.2 Inside the gates: TTL, PMOS, NMOS and CMOS

Key ideas

- Standard TTL NAND: multi-emitter input transistor, phase splitter and totem-pole output.
- Open-collector outputs need a pull-up resistor and can be joined (wired-AND).
- CMOS inverter: a P-MOSFET to Vdd and an N-MOSFET to ground; one of them is always off, so almost no current flows when idle.
- CMOS NAND: two P-MOSFETs in parallel to Vdd and two N-MOSFETs in series to ground.

9.2.1 Basic

Explain how a CMOS inverter works for input 0 and input 1.

YOUR ANSWER

Write your answer here, then compare it with the answer.

9.2.2 Practice

In a 2-input CMOS NAND gate, which transistors are on when A = 1 and B = 0? What is the output?

YOUR ANSWER

output number

9.2.3 Practice

Why must unused CMOS inputs never be left floating?

YOUR ANSWER

Write your answer here, then compare it with the answer.

9.2.4 Practice

What is a totem-pole output? Why must two totem-pole outputs never be connected together?

YOUR ANSWER

Write your answer here, then compare it with the answer.

9.2.5 Challenge

Three open-collector outputs are joined to one pull-up resistor. What logic function does the joined wire give?

YOUR ANSWER

function answer

Chapter 10

Introduction to control systems

Transducers, sensors, actuators, and open-loop versus closed-loop control.

10.1 Transducers, sensors and actuators

Key ideas

- A transducer changes one form of energy into another.
- A sensor (input transducer) measures a physical quantity and gives an electrical signal.
- An actuator (output transducer) turns an electrical signal into action: movement, heat, light, sound.

10.1.1 Basic

Sort these into sensors and actuators: thermistor, DC motor, LDR, solenoid valve, microphone, loudspeaker, push-button, relay, ultrasonic sensor, heater.

YOUR ANSWER

sensors e.g. a, b, c actuators e.g. a, b, c

10.1.2 Basic

Give the energy change made by: (a) a microphone (b) a loudspeaker (c) a solar cell (d) an LED (e) a thermocouple.

YOUR ANSWER

Write your answer here, then compare it with the answer.

10.1.3 Practice

Choose a sensor for each job: (a) detect a person in a room (b) measure the level of water in a tank (c) count bottles on a conveyor (d) measure motor speed.

YOUR ANSWER

Write your answer here, then compare it with the answer.

10.1.4 Practice

What is the difference between an analogue and a digital sensor? Give one example of each.

YOUR ANSWER

Write your answer here, then compare it with the answer.

10.2 Open-loop and closed-loop control

Key ideas

- A control system has an input (set point), a controller, an actuator and the process (plant) being controlled.
- Open loop: no measurement of the output; the controller cannot correct errors.
- Closed loop: a sensor feeds the output back; the controller compares it with the set point (error = set point – feedback) and corrects it.

10.2.1 Basic

Say whether each system is open-loop or closed-loop: (a) a toaster with a timer (b) an oven thermostat (c) a washing machine that runs a fixed program (d) a car's cruise control (e) traffic lights on a timer (f) a water tank with a float valve.

YOUR ANSWER

(a) answer (b) answer

(c) answer (d) answer

(e) answer (f) answer

10.2.2 Basic

Draw (describe) the block diagram of a closed-loop temperature control system and name each block.

YOUR ANSWER

Write your answer here, then compare it with the answer.

10.2.3 Practice

Give two advantages and two disadvantages of closed-loop control compared with open-loop.

YOUR ANSWER

Write your answer here, then compare it with the answer.

10.2.4 Practice

A room heater has its set point at 22 °C. The sensor reads 19 °C. What is the error and what does the controller do?

YOUR ANSWER

error e.g. 1.5 k°C

10.2.5 Challenge

Why does a simple ON/OFF thermostat use a small dead band (hysteresis), e.g. ON below 21.5 °C and OFF above 22.5 °C?

YOUR ANSWER

Write your answer here, then compare it with the answer.

Chapter 11

Sequential function charts (SFC / GRAFCET)

Steps, transitions and actions; action qualifiers; and the rules for serial, selection and parallel branches.

11.1 Steps, transitions and actions

Key ideas

- A step is a stable state of the machine; the initial step has a double square. An active step has a token.
- A transition sits between two steps and has a condition (receptivity). It fires when the step before it is active and its condition is true.
- Actions are written in a rectangle beside the step. Qualifiers: N (while active), S (set, stored), R (reset), L (time limited), D (delayed), P (pulse).

11.1.1 Basic

What do these SFC symbols mean: a double square, a single square, a short horizontal bar on a link, a rectangle beside a step?

YOUR ANSWER

Write your answer here, then compare it with the answer.

11.1.2 Basic

Give the meaning of the action qualifiers N, S, R, L, D and P.

YOUR ANSWER

Write your answer here, then compare it with the answer.

11.1.3 Practice

A press works like this: when the start button S is pressed, the ram goes down (DOWN) until the low limit switch L1; then it goes up (UP) until the high limit switch L0; then it waits for the next start. Write the SFC.

YOUR ANSWER

Write your answer here, then compare it with the answer.

11.1.4 Practice

A mixer tank: press START → open valve V1 until the level sensor H is reached → run the mixer M for 30 s → open the drain valve V2 until the low sensor B → back to the start. Write the SFC with the timer.

YOUR ANSWER

Write your answer here, then compare it with the answer.

11.1.5 Challenge

Why does an action with the S qualifier need a later step with the R qualifier?

YOUR ANSWER

Write your answer here, then compare it with the answer.

11.2 Rules of evolution: serial, selection and parallel branches

Key ideas

- Serial: steps follow each other one by one.
- Selection (OR) branch: a single horizontal line; only one of the paths is taken, the one whose transition is true first. Conditions should exclude each other.
- Parallel (AND) branch: a double horizontal line; all paths start together, and the chart only continues when every path has finished (synchronisation).
- A transition fires when (1) all the steps before it are active and (2) its condition is true. Firing deactivates the steps before and activates the steps after it, at the same moment.

11.2.1 Basic

What is the difference between a selection branch and a parallel branch in an SFC? How are they drawn?

YOUR ANSWER

Write your answer here, then compare it with the answer.

11.2.2 Practice

A sorting machine measures a box: if it is big (G) it pushes it left (PL); if it is small (G') it pushes it right (PR); then it returns to waiting. Draw the SFC with a selection branch.

YOUR ANSWER

Write your answer here, then compare it with the answer.

11.2.3 Practice

A machine must drill (step D) and polish (step P) at the same time; when both are finished it unloads the part. Which kind of branch do you use and when does the unload step start?

YOUR ANSWER

Write your answer here, then compare it with the answer.

11.2.4 Challenge

Steps 4 and 7 are active. The transition after them (with a double line) has the condition ‘ready’ = 1. Step 5 is not active. Which steps are active after the transition fires if it leads to step 8?

YOUR ANSWER

active step(s) after firing e.g. a, b, c

Chapter 12

Programmable logic controllers (PLC)

What a PLC is, how it scans its program, and programming in ladder logic, statement list and function blocks.

12.1 PLC structure and operation

Key ideas

- A PLC is an industrial computer: power supply, CPU, memory, input modules, output modules and a programming device.
- Scan cycle: 1) read all inputs, 2) run the program, 3) update all outputs, 4) housekeeping/communication, then repeat.
- Advantages over relay logic: easy to change, fewer wires, fault finding, timers and counters built in, small size.

12.1.1 Basic

Name the main parts of a PLC and say what each one does.

YOUR ANSWER

Write your answer here, then compare it with the answer.

12.1.2 Basic

Describe the four steps of the PLC scan cycle.

YOUR ANSWER

Write your answer here, then compare it with the answer.

12.1.3 Practice

A PLC has a scan time of 10 ms. A push-button is pressed for only 4 ms. Can the PLC miss it? Explain.

YOUR ANSWER

can it miss it? (yes/no) answer

12.1.4 Basic

Give four advantages of a PLC over hard-wired relay control.

YOUR ANSWER

Write your answer here, then compare it with the answer.

12.2 Ladder logic

Key ideas

- The left rail is the power line. A rung is read from left to right; rungs are read from top to bottom.
- —| |— normally open contact (true when the input is 1). —|/|— normally closed contact (true when the input is 0). —( )— output coil.
- Contacts in series = AND. Contacts in parallel = OR.
- A seal-in (latching) contact keeps a motor running after the start button is released.

12.2.1 Basic

Draw the ladder rung for Y = A·B (AND) and for Y = A + B (OR).

YOUR ANSWER

Write your answer here, then compare it with the answer.

12.2.2 Basic

Draw the ladder rung for Y = A' (NOT) and for Y = A·B'.

YOUR ANSWER

Write your answer here, then compare it with the answer.

12.2.3 Practice

Draw a motor start/stop circuit with a seal-in contact. START is a normally open button I0.0, STOP a normally closed button I0.1, the motor M is Q0.0.

YOUR ANSWER

Write your answer here, then compare it with the answer.

12.2.4 Practice

Write the ladder rung for Y = (A + B)·C'.

YOUR ANSWER

Write your answer here, then compare it with the answer.

12.2.5 Practice

Write the ladder rung for an XOR: Y = A·B' + A'·B.

YOUR ANSWER

Write your answer here, then compare it with the answer.

12.2.6 Practice

Write the statement list (STL) for the start/stop rung with seal-in (Siemens style).

YOUR ANSWER

Write your answer here, then compare it with the answer.

12.2.7 Challenge

A tank pump P must run when the low-level switch L is ON and must stop when the high-level switch H turns ON. It must keep running between the two levels. Write the ladder logic.

YOUR ANSWER

Write your answer here, then compare it with the answer.

12.2.8 Challenge

Two buttons A and B must both be pressed (two-hand safety control) to start a press, and a light curtain C (1 = clear) must be clear. Write the logic and the ladder rung.

YOUR ANSWER

PRESS = e.g. AB' + C

12.2.9 Practice

Name the three common PLC programming languages besides ladder logic and explain function block diagrams (FBD) briefly.

YOUR ANSWER

Write your answer here, then compare it with the answer.

12.2.10 Practice

An ON-delay timer T1 has a preset of 5 s and is enabled by input I0.2. Describe what output Q0.1 (driven by the timer’s done bit) does when I0.2 is switched on for 3 s and then for 8 s.

YOUR ANSWER

Write your answer here, then compare it with the answer.

Chapter 13

Mixed revision test

Exam-style questions that mix every chapter. Try them without looking back, then check your answers.

13.1 Part A: short questions

13.1.1 Basic

Convert $(222)_{10}$ to binary, octal, hexadecimal and BCD.

YOUR ANSWER

binary: binary, e.g. 1011 | octal: octal | hex: hex, e.g. 3F | BCD: e.g. 0110

13.1.2 Basic

Write −58 in 8-bit 2's complement.

YOUR ANSWER

8 bits: e.g. 0110

13.1.3 Basic

Give the Gray code of 1100_2.

YOUR ANSWER

Gray code e.g. 0110

13.1.4 Basic

Which two gates are called universal gates and why?

YOUR ANSWER

the two gates e.g. a, b, c

13.1.5 Basic

How many select lines does a 64-to-1 multiplexer need?

YOUR ANSWER

select lines number

13.1.6 Basic

What is the frequency at the output of the 4th flip-flop of a ripple counter clocked at 48 kHz?

YOUR ANSWER

frequency e.g. 1.5 kHz

13.1.7 Basic

How many states does a 6-bit Johnson counter have?

YOUR ANSWER

states number

13.1.8 Basic

Is a street light switched on by a light sensor at dusk an open-loop or a closed-loop system? Explain.

YOUR ANSWER

open or closed loop? answer

13.2 Part B: longer problems

13.2.1 Practice

Simplify F(A, B, C, D) = Σm(0, 1, 4, 5, 6, 7, 12, 13) with a K-map. Give the SOP and the POS forms.

YOUR ANSWER

SOP: F = e.g. AB' + C POS: F = e.g. AB' + C

13.2.2 Practice

Design a circuit that compares two 2-bit numbers A = A1A0 and B = B1B0 and gives G = 1 when A > B.

YOUR ANSWER

G = e.g. AB' + C

13.2.3 Practice

A 555 astable has RA = 2.2 kΩ, RB = 4.7 kΩ and C = 47 nF. Find the frequency and the duty cycle.

YOUR ANSWER

frequency e.g. 1.5 kHz duty cycle e.g. 1.5 k%

13.2.4 Challenge

Design a synchronous MOD-6 counter (0 → 5) with D flip-flops.

YOUR ANSWER

D2 = e.g. AB' + C D1 = e.g. AB' + C

D0 = e.g. AB' + C

13.2.5 Practice

Write the truth table and the simplest expression for a circuit with three inputs whose output is 1 when exactly one input is 1.

YOUR ANSWER

Y = e.g. AB' + C

13.2.6 Practice

A 4-bit shift-left register holds 0110. 1, 1, 0 are shifted in at the right. Give the contents after each pulse.

YOUR ANSWER

pulse 1 e.g. 0110 pulse 2 e.g. 0110

pulse 3 e.g. 0110

13.2.7 Challenge

Draw the SFC and the ladder logic for a garage door: button B opens it (OPEN) until the top switch T; after 10 s it closes (CLOSE) until the bottom switch D; a light beam L (1 = blocked) during closing makes it open again.

YOUR ANSWER

Write your answer here, then compare it with the answer.

13.2.8 Practice

Compare TTL and CMOS: fill in the table.

YOUR ANSWER

Write your answer here, then compare it with the answer.

Notation: A' means NOT A (A with a bar), · or writing letters together means AND, + means OR, ⊕ means XOR and ⊙ means XNOR. Σm lists the minterms (rows where the output is 1), ΠM the maxterms (rows where it is 0).